Microwave Variable-Gain Amplifier with Dual-Gate GaAs FET

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Abstract—**An encapsulated dual-gate GaAs Schottky barrier gate FET has been characterized with an equivalent circuit representation. The second gate bias dependence of the transconductance has suggested that the FET can be used as a variable-gain amplifying device at microwave frequencies. The experiments on the variable-gain amplifiers with the dual-gate GaAs FET's have exhibited the following. 1) Broad-band amplification can be achieved by adopting a stagger tuning technique, although the Q's of the input and output of the GaAs FET are much higher than those of the Si bipolar transistor. 2) The gain can be controlled only by the second gate bias voltage without degradation of bandpass performance. The results have shown the feasibility of the dual-gate GaAs FET for a microwave variable-gain amplifier.**

I. INTRODUCTION

RECENTLY, the single-gate GaAs Schottky barrier gate FET has attracted considerable attention because of its lower noise performance at microwave frequencies as well as its higher maximum oscillation frequency compared to the Si bipolar transistor. Particularly above 6 GHz, the GaAs FET should dominate low noise application [1]. Furthermore, the GaAs FET is also promising as a microwave multifunction device with a dual-gate structure. One of the attractive functions is a gain control characteristic which is not available in the Si bipolar transistor. Of course, the Si metal–oxide–semiconductor (MOS) tetrode exhibits almost the same characteristics, but operates only at about one order magnitude lower frequencies than the dual-gate GaAs FET.

On the other hand, the most usual microwave amplifiers are constructed with Si bipolar transistors and, for use in automatic gain control (AGC) circuits, need variable attenuators with p-i-n diodes. The gain of the dual-gate GaAs FET, however, can easily be varied only by the second gate bias voltage. Therefore, not only can the circuit construction be simplified, but also the power dissipation can be decreased by using dual-gate GaAs FET's in microwave variable-gain amplifiers for AGC circuits.

The purpose of this paper is to show the feasibility of the dual-gate GaAs FET for a microwave variable-gain amplifier. First, a dual-gate GaAs FET is characterized with an equivalent circuit representation. Then the circuit design of the amplifier and the performances of two experimental amplifiers are described to illustrate the design concept.

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II. CHARACTERIZATION OF DUAL-GATE GaAs FET

The schematic structure of the dual-gate GaAs FET used is shown in Fig. 1(a), along with the electrode dimensions and separations. The electrodes are about 300 μm in width. The FET pellet is encapsulated in a ceramic package with a diameter of 1.8 mm. The design and performance of the dual-gate GaAs FET, including the effect of the package parasitics, have been described in detail elsewhere [2], [3]. The S-parameter measurements have shown that the maximum unilateral transducer gain G_{max} of the dual-gate GaAs FET is about 20 dB at 2 GHz. Although the gain is about 2 dB lower than that of the single-gate GaAs FET with almost the same electrode dimensions, the stability factor is much higher because of the existence of the second gate grounded for RF.

In this paper, the encapsulated dual-gate GaAs FET is characterized with an equivalent circuit representation for design convenience. The frequency characteristics of the Y-parameters, which can easily be calculated from the S-parameters, have exhibited the property that the encapsulated dual-gate GaAs FET working at the frequencies below about 3 GHz can be represented by an equivalent circuit shown in Fig. 1(b). At higher frequencies, the equivalent circuit becomes more complicated, since the package parasitics affect the characteristics of the device. Therefore, the measured data should preferably be used for the design of the amplifier operated at above 3 GHz or more. It should be noted that the preceding discussion is for the case of using the encapsulated FET.

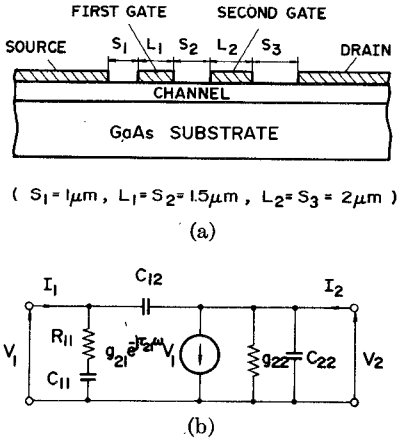

Fig. 1. (a) Schematic structure of dual-gate GaAs FET. (b) Simplified equivalent circuit.

The gain control characteristic of the dual-gate GaAs FET is due to the fact that the transconductance g_{21} can be varied by adjusting the gate bias voltage. Fig. 2(a) and 2(b) show the transconductances as functions of the first and second gate bias voltages, respectively. Although the transconductance can be varied by the first gate bias voltage as well as the second gate bias voltage, it does not monotonically change with the first gate bias and reaches a maximum, as shown in Fig. 2(a). On the other hand, the transconductance decreases with the second gate bias voltage within the specified range shown in Fig. 2(b). Therefore, the second gate bias dependence of the transconductance can be preferably used for a variable-gain amplifier in the AGC circuit.

Fig. 3 shows the equivalent circuit parameters except for g_{21} and τ_{21} as a function of the second gate bias voltage. In order to apply the dual-gate GaAs FET to a broad-band variable-gain amplifier, the equivalent circuit parameters, except for g_{21}, should not vary with the second gate bias voltage. This requirement is satisfied by the capacitances C_{11}, C_{12}, and C_{22} as shown in Fig. 3. On the other hand, resistive components R_{11} and g_{22} vary with the second gate bias voltage, but have little effect on the amplifier performance as shown later.

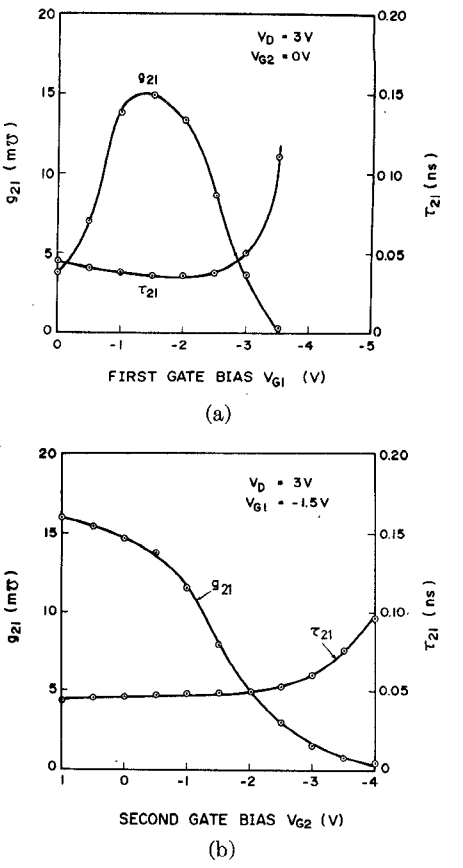

Fig. 2. (a) Measured transconductance and delay time as a function of the first gate bias voltage. (b) As a function of the second gate bias voltage.

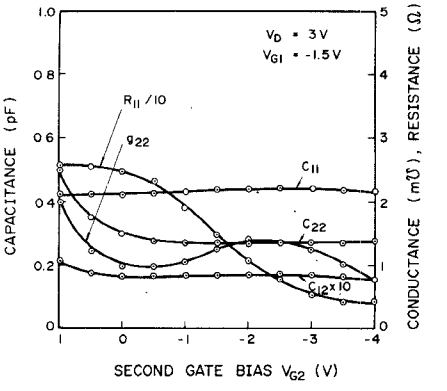

Fig. 3. Measured equivalent circuit parameters as a function of second gate bias voltage.

III. CIRCUIT DESIGN OF AMPLIFIER

A. Design Consideration

One of the important applications of microwave variable-gain amplifiers is in the millimeter-wave radio relay system [4]. Since in the system the receiving power is strongly affected by the weather conditions, the gain of the IF amplifier should be automatically controlled to give a constant output power. At the same time, broad-band amplification, e.g., 420 MHz centered at 1.7 GHz, is required for the high-speed phase-shift keyed (PSK) repeater system.

Since the Si bipolar transistor exhibits relatively low Q's for both input and output of the device, the broad-band characteristics can easily be realized by usual matching techniques. For instance, the Q's of the encapsulated Si bipolar transistor, HP35862E, are $0.4 \sim 0.6$ for both input and output at 1.7 GHz. On the other hand, the Q's of the dual-gate GaAs FET are $15 \sim 20$ for the input and $3 \sim 5$ for the output at the same frequency. These high-Q characteristics cause difficulties in the design of a broad-band amplifier with the dual-gate GaAs FET's.

B. Circuit Construction

Fig. 4 shows a schematic diagram of a typical multistage amplifier. For conventional broad-band multistage amplifiers with Si bipolar transistors, every interstage coupling network is usually designed to yield a flat gain in the desired passband. It is difficult, however, to apply this design concept to broad-band multistage amplifiers

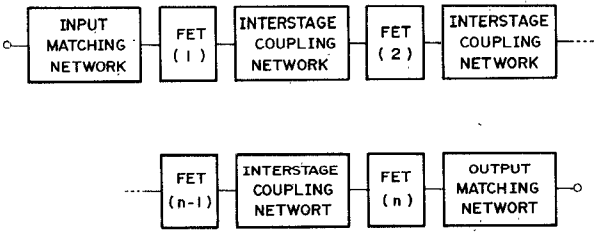

Fig. 4. Schematic diagram of typical multistage amplifier.

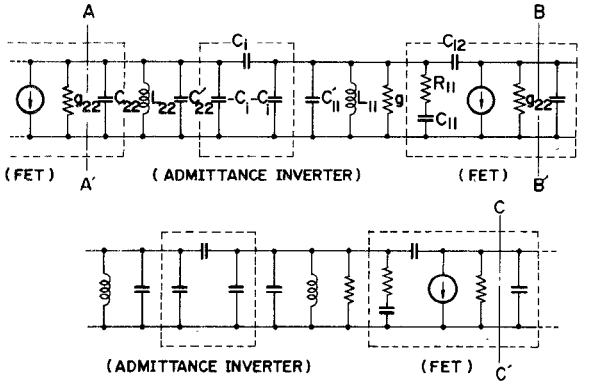

Fig. 5. Interstage coupling networks for variable-gain amplifier with dual-gate GaAs FET's.

with dual-gate GaAs FET's because of their high-Q values. Therefore, a stagger tuning technique of combining two FET's, each of which has adequate gain at either high- or low-frequency region in the desired passband, has been adopted.

The interstage coupling network has been constructed by taking into account the following.

1) Since it is not necessary to broaden every stage, single-tuned shunt circuits are employed for both input and output of every FET. The tuning inductor in the shunt resonant circuit can also be used to feed the bias voltage of the FET.

2) Every FET, including its input and output shunt resonant circuits, is connected in cascade through an admittance inverter, which is used to set the impedance level and also to block the dc bias.

3) In the input of every FET, a shunt conductance is added to enhance the stability of the circuit and also to adjust the peak value of the gain.

Fig. 5 shows the interstage coupling networks, in which the section from AA' to CC' is considered as a unit amplifier section. If the unit amplifier section can be designed to yield a flat gain, the multistage amplifier composed of multiple unit amplifier sections will give a flat bandpass response.

The resonant frequencies of the former (AA'–BB') and latter (BB'–CC') stages are chosen at lower and higher frequencies, respectively, in the desired passband. Tuning inductors are determined from those resonant frequencies, i.e.,

$$f_r = \frac{1}{2\pi L_{22}(C_{22} + C_{22}')} = \frac{1}{2\pi L_{11}(C_{11} + C_{11}')}. \quad (1)$$

The negative capacitances in the admittance inverter are cancelled out by C_{11}' and C_{22}'. If C_{11}' and C_{22}' are chosen so as to be equal to C_i, additional shunt capacitors can be eliminated in the circuit.

C. Circuit Design

Fig. 6 illustrates a schematic diagram of an amplifier used to confirm the function of the unit amplifier section. The input of the single-gate GaAs FET used in the first

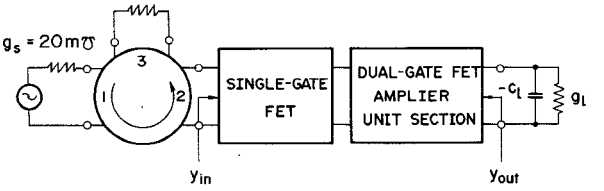

Fig. 6. Schematic diagram of the amplifier used to confirm the function of unit amplifier section.

stage, whose equivalent circuit parameters are quite similar to those of the dual-gate GaAs FET used in the latter stages, is directly connected to a 50-Ω transmission line through a circulator. Since the input impedance of the single-gate GaAs FET is sufficiently high in the frequency range under consideration, at least below 2 GHz, compared with a characteristic impedance of 50 Ω, the input of the device scarcely affects the bandpass performance of the unit amplifier section. Fig. 7 shows the calculated performance of the amplifier of Fig. 6, assuming an ideal tuning circuit for the output. In the calculation, the parameters f_r, C_i, and g are chosen as follows. f_r = 1.3 GHz, C_i = 0.07 pF, g = 0.5 mmho for the former stage; f_r = 2.1 GHz, C_i = 0.07 pF, g = 3.0 mmho for the latter stage.

It is seen from Fig. 7 that a 1-dB bandwidth of about 700 MHz at 20-dB gain is theoretically achievable with a unit amplifier section. The input admittance y_{in} indicates complicated frequency characteristics because of feedthrough capacitances C_{12} of the FET's, but the output admittance y_{out} can be represented by a simple RC circuit.

In order to examine the amplifier experimentally, a broad-band impedance transforming network is required for the output. Fig. 8 shows a double-tuned impedance transforming network adopted for the experimental amplifier. Here the constant $n(>1)$ is the transforming ratio and C is an arbitrary value of capacitance. From the realizability of the network, the negative capacitances $-C$ and $-n^2C/(n-1)$ should be cancelled out by the adjacent circuits. For this purpose, a series resonant circuit is added between the ideal transformer and the load conductance g_2. If the following condition is satisfied, the output circuit can be realized.

$$C_1 \leq \frac{n^2}{n-1} C. \quad (2)$$

The reflection coefficient Γ looking into the load from the output conductance g_0 is given by

$$|\Gamma|^2 = \left| \frac{(-1 + jQ_0x)(1 + jQ_1x) + k}{(1 + jQ_0x)(1 + jQ_1x) + k} \right|^2$$

$$\simeq \left(\frac{k-1}{k+1}\right)^2 (1 + ax^2) \quad (3)$$

where

$$x = \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}$$

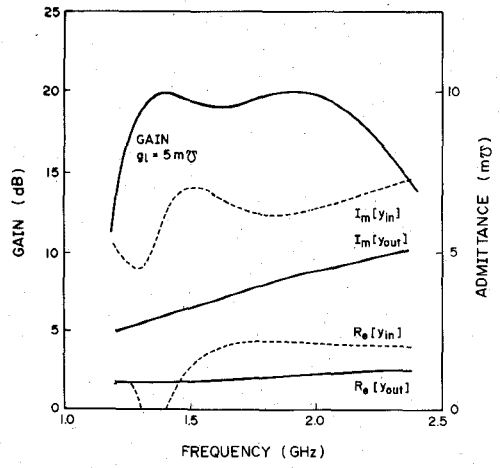

Fig. 7. Calculated performance of the amplifier shown in Fig. 6.

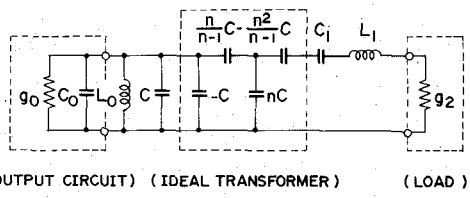

Fig. 8. Double-tuned impedance transforming network for the output.

$$Q_0 = \frac{\omega_0(C_0 + C)}{g_0}$$

$$Q_1 = g_2\omega_0 L_1$$

$$k = \frac{g_2}{n^2 g_0}$$

and a is expressed by

$$a = \frac{2Q_0Q_1}{k+1} - \frac{2Q_0Q_1}{k-1} + \frac{(Q_0 - Q_1)^2}{(k-1)^2} - \frac{(Q_0 + Q_1)^2}{(k+1)^2}. \quad (4)$$

Apparently from (3) and (4), the approximate maximally flat bandpass response can be achieved by choosing Q_1 so that (4) is equal to zero.

IV. EXPERIMENTAL RESULTS

A. Amplifier Fabrication

To illustrate the design of the broad-band variable-gain amplifier with dual-gate GaAs FET's, two experimental amplifiers were realized. These amplifiers were fabricated on alumina substrates by using lumped elements. The shielded coplanar waveguide was employed for the fundamental structure of the transmission line. As lumped elements, spiral inductors and interdigital capacitors were used for tuning inductors and coupling capacitors in the admittance inverters, respectively. The inductances of the spiral inductors were in a range between 7 and 20 nH. Although the spiral conductors were 50 μm wide and 50 μm apart, the sizes became appreciable because of the large inductances. Therefore, the parasitic capacitances

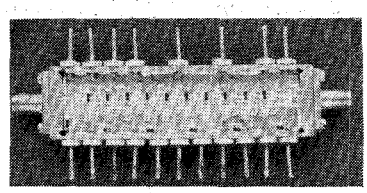

Fig. 9. Photograph of the experimental multistage amplifier composed of five unit amplifier sections.

due to distributed line effects could not be neglected even at 1.7 GHz and were considered in the design [5]. Chip resistors were employed in the input of every FET to facilitate replacement during adjustments, and beam-lead capacitors were employed for RF bypass. Fig. 9 shows an experimental amplifier composed of five unit amplifier sections.

B. Performance of the Unit Amplifier Section

Fig. 10 shows measured bandpass performances of the experimental unit amplifier section for different values of the second gate bias voltages. From 1.25 to 2.05 GHz, i.e., over 50-percent bandwidth, an 18-dB gain with less than 1-dB deviation was obtained at the second gate bias of 0 V. The measured bandpass performance is quite similar to the calculated one shown in Fig. 7. With regard to gain control, it should be noted that neither center frequency nor bandpass performance fluctuates over a 35-dB change due to the second gate voltage changes.

The gain control characteristic is due to the change of the transconductance depending on the second gate bias voltage adjustment. Since the transducer gain G_t of the unit amplifier section is given in terms of the Y parameters y_{ij} $(i = 1,2; j = 1,2)$ of the unit amplifier section by

$$G_t = \frac{4\,\mathrm{Re}\,[y_S]\,\mathrm{Re}\,[y_L]\,|\,y_{21}\,|^2}{|\,(y_{11} + y_S)(y_{22} + y_L) - y_{12}y_{21}\,|^2} \quad (5)$$

where y_S and y_L are the source and load admittances, respectively. Since the parameter y_{21} is expressed in terms of the Y parameters of the former and latter stages $y_{ij}^{(1)}$ and $y_{ij}^{(2)}$ $(i = 1,2; j = 1,2)$ by

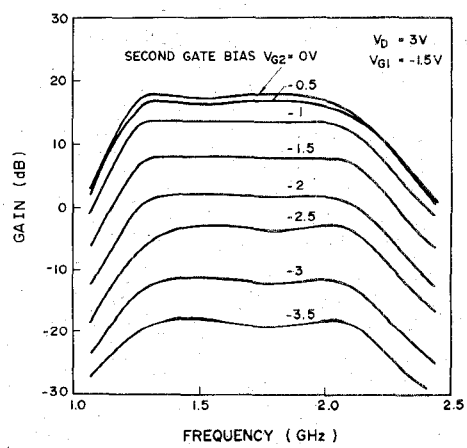

Fig. 10. Bandpass performance of the experimental unit amplifier section for different values of second gate bias voltage.

$$y_{21} = \frac{y_{21}^{(1)} y_{21}^{(2)}}{y_{22}^{(1)} + y_{11}^{(2)}} \qquad (6)$$

the gain G_t changes proportionally with $g_{21}{}^4$. Similarly, the gain of the multistage amplifier composed of m unit amplifier sections is proportional to $g_{21}{}^{4m}$. Fig. 11 compares measured and calculated gain reduction characteristics, and shows good agreement. The calculation was performed by using the second gate bias dependence of the transconductance g_{21} shown in Fig. 2(b).

C. Multistage Amplifier Performance

The experimental multistage amplifier is composed of a single-gate GaAs FET for the first stage and five unit amplifier sections with the dual-gate GaAs FET's, as shown in Fig. 9. Here a circulator is assumed in the input of the amplifier. The output impedance transforming network is almost the same as that of the experimental unit amplifier section. Fig. 12 shows measured bandpass performances of the experimental multistage amplifier, from which it is seen that a 3-dB bandwidth of 480 MHz at a midband gain of 60 dB is obtained at the second gate bias of 0 V. The gain per unit amplifier section was reduced compared to the experimental unit amplifier section, since a larger value of conductance g was added to the input of every FET in order to enhance the stability. It is also seen from Fig. 12 that the gain of the amplifier is controlled only by the second gate bias voltage without degradation of bandpass performance. From these experimental results, it is concluded that the dual-gate GaAs FET can be utilized as a variable-gain amplifying device at microwave frequencies.

V. CONCLUSION

A dual-gate GaAs Schottky barrier gate FET has been characterized with an equivalent circuit representation. The circuit design of the broad-band amplifier with the dual-gate GaAs FET's, the design realization, and the performances of the experimental amplifiers have been described. The second gate bias dependence of the transconductance has suggested that the FET can be used as a variable-gain amplifying device at microwave frequencies. Although the Q's of the input and output of the dual-gate GaAs FET are more than ten times higher than those of the Si bipolar transistor, broad-band multistage amplifiers have been realized by adopting a stagger tuning technique. Furthermore, the gains of the amplifiers have been controlled only by the second gate bias voltages without degradation of bandpass performances. Those experimental results have shown the feasibility of the dual-gate GaAs FET for a microwave variable-gain amplifier.

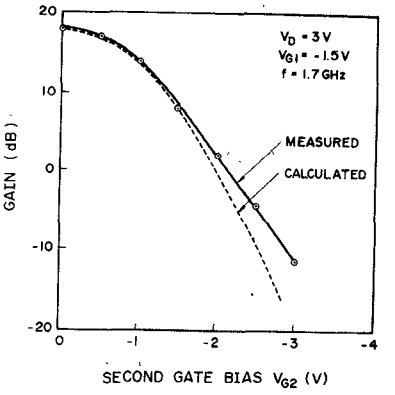

Fig. 11. Measured and calculated gains as a function of second gate bias as voltage.

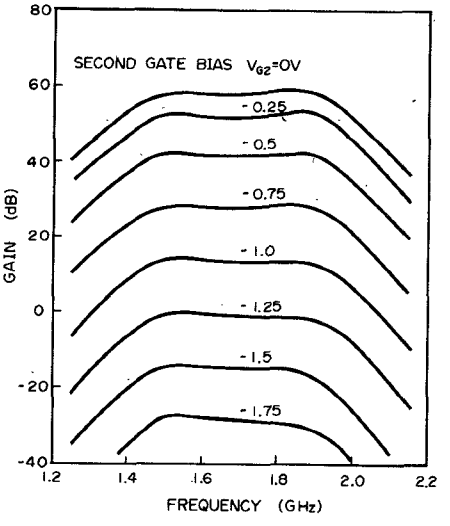

Fig. 12. Bandpass performance of the experimental multistage amplifier.

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